## IN THE SPECIFICATION

Please amend the paragraph page 13, lines 15-25 in the manner noted below. The amendment is believed to introduce no new matter.

FIG. 5 illustrates a circuit implementing the traceback for the trellis section in accordance with one embodiment of the present invention. Trace registers 510-517 are clocked storage registers which correspond to states 0-7. In this example, they are representative of the bit values held in the various nodes, such as depicted in the trellis diagram of FIG. 4B. As indicated in the traceback diagram, these states will feed the previous states. For example, next state 4 will feed either previous state 0 or 1, depending upon which of the two states (0 or 1) had the previous best metric. In like manner, the output of register 514 (state 4) is hardwired to the multiplexers ~~multiplexors~~ ("muxes") (520, 521) for states 0 and 1. Through the use of clocked trace registers and data selection blocks (e.g. muxes), in one example, the circuit of FIG. 5, evaluated over several clock cycles, is used to perform the traceback function defined by a Viterbi trellis.

Please amend the paragraph page 19, lines 3-15 in the manner noted below. The amendment is believed to introduce no new matter.

The methods and apparatus described above may be used to implement a Viterbi decoder in a minimized hardware configuration. Although the configurations have been described in the context of multiplexers ~~multiplexors~~ and trace registers, the present invention is not limited to the use of such hardware. The invention is equally applicable to configuration using other data selection blocks and other trace or storage registers such as but not limited to flip flops, other types of registers, memory devices, and /or configured programmable logic devices. It should be understood that the principals of the present invention in all of its embodiments may also be extended to include implementation in programmable logic devices in a variety of ways and including the use of look-up tables to perform logic functions. The present invention is intended to cover all such embodiments. The descriptions above are also not limited to a single encoding rate. The embodiments of this invention are expandable to all code rates k/n, where k may be greater than 1.

Please amend the Abstract in the manner noted below. The amendment is believed to introduce no new matter.

Methods and apparatus are provided for efficiently implementing a traceback decoding of Viterbi codes. A Viterbi decoder circuit having at least two data selection blocks and at least two trace registers is described. ~~, t~~The number of registers corresponds ~~corresponding~~ to the number of states in a Viterbi trellis diagram applicable to encoded data. The trace registers are used to represent the current state best metric and are each configured to send their output to the inputs of the predecessor states representing the possible branches to the current state. The best metric for the predecessor state is determined using a survivor vector stored in memory. Traceback occurs by sequentially reading survivor vectors from memory, using the vectors to control the data selection blocks, and using the trace registers to sequentially identify predecessor states in the traceback.